

Design for Power Integrity: Decap Selection Strategies for Low Target Impedance

Milan Pavlović, Andrey Shadrin

Abstract – The scaling of CMOS technology to nanometer nodes has pushed Power Distribution Network (PDN) design into a critical regime where supply voltages drop below 1.0 V and dynamic currents exceed hundreds of amperes. To maintain voltage stability, the target impedance (Z_{target}) has plummeted to sub-milliohm levels, rendering traditional bulk capacitance strategies obsolete. This paper critically examines the phenomenon of PCB package resonance, a dominant limiting factor in modern high-speed systems. We evaluate advanced mitigation techniques, including inductance decomposition, genetic algorithm (GA) optimization, and the pole-zero (P&Z) matching method. Furthermore, we analyze the efficacy of emerging Reversed Aspect Ratio (LW) capacitors and demonstrate that a "package-aware" co-design methodology is mandatory to avoid gross overdesign. The findings confirm that optimizing for controlled damping, rather than minimum impedance, is the only viable path to robust power integrity.

Keywords - Power Integrity (PI), Power Distribution Network (PDN), Decoupling Capacitors, Target Impedance.

I. INTRODUCTION

The fundamental objective of Power Integrity (PI) is to maintain the voltage at the integrated circuit (IC) pads within a tight tolerance (typically $\pm 2\%$) despite rapid di/dt transients^[1]. In high-speed computing, the PDN transforms from a lumped DC supply into a distributed transmission line network characterized by frequency-dependent impedances. The design goal is defined by the target impedance (Z_{target}):

$$Z_{\text{target}} = \frac{V_{\text{DC}} * \text{Noise Margin}}{I_{\text{AC}}} \quad (1)$$

With I_{AC} transients exceeding 100A, Z_{target} values of 0.1 mΩ to 5 mΩ are standard. Achieving this requires a flat impedance profile across a bandwidth from DC to the GHz range. However, the inductive nature of interconnects creates impedance peaks (anti-resonances) when interacting with capacitive stages. Recent literature challenges the traditional "low and flat" dogma, suggesting that aggressively lowering Equivalent Series Resistance (ESR) can inadvertently increase the Quality Factor (Q) of system resonances, leading to higher noise amplitudes^[2]. This investigates strategies for selecting decoupling capacitors to suppress these resonances, specifically focusing on the critical interface between the PCB and IC.

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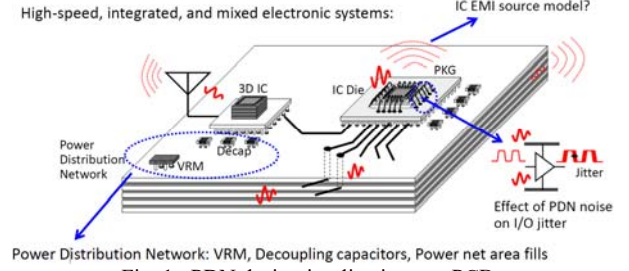


Fig. 1. PDN design implications on PCBs

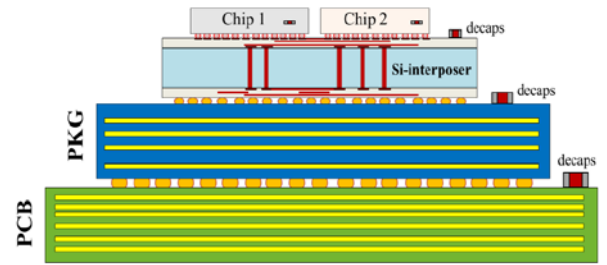


Fig. 2. Hierarchical PDN structure

II. THEORETICAL FRAMEWORK OF INDUCTANCE

High-speed PDN design is governed by Maxwell's equations, often approximated using Partial Element Equivalent Circuits (PEEC). A critical distinction exists between loop inductance (L_{loop}), which depends on the entire current path geometry, and partial inductance, a mathematical construct useful for matrix modeling. For capacitor selection, the mounting loop inductance is paramount. It determines the effectiveness of a capacitor above its self-resonant frequency (SRF), where it acts purely as an inductor. Inductance decomposition to systematically lower PDN impedance, the total inductance seen by the die is decomposed into three quantifiable components:

1. $L_{\text{PCB_IC}}$ (Vertical Interconnect): The inductance of BGA balls and vias connecting the IC to internal planes. This is often the dominant high-frequency limiter.
2. $L_{\text{PCB_EQ}}$ (Plane Spreading): The lateral inductance of the power/ground plane pair is inversely proportional to the dielectric thickness.
3. L_{above} (Mounting Inductance): The parallel combination of all decoupling capacitors and their mounting geometries (pads, traces, vias)^[3].

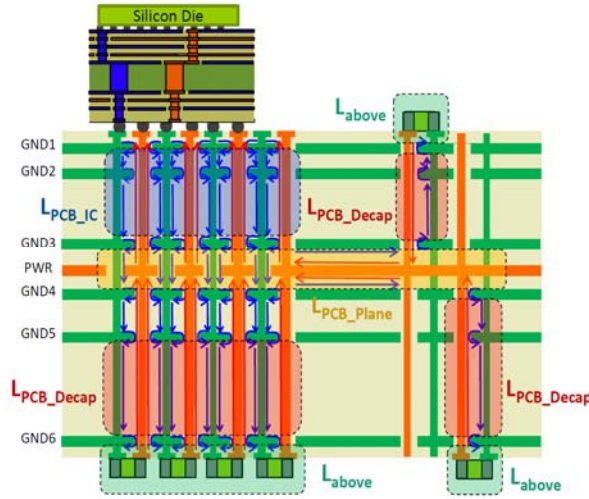


Fig. 3. Inductance Decomposition

The profound concept derived from this decomposition is the "Physical Limit" of the board. If every available capacitor location is shorted to ground (0Ω , $0H$), the impedance is still limited by the parallel combination of the mounting inductances (L_{mount}) and the vertical interconnects ($L_{\text{PCB_IC}}$).

$$Z_{\text{limit}}(\omega) = j\omega (L_{\text{PCB_IC}} \parallel L_{\text{above_min}}) \quad (2)$$

If $Z_{\text{limit}} > Z_{\text{target}}$ at any frequency, the design is structurally unfeasible. No capacitor selection can resolve this, only stack-up changes (e.g., thinner dielectrics, shallower planes) can lower the physical limit.

III. ALGORITHMIC SELECTION METHODOLOGIES

Once physical feasibility is established, selecting the optimal capacitor mix is nontrivial. Genetic Algorithm (GA) vs. Pole-Zero (P&Z). Genetic Algorithms are stochastic search methods that evolve a population of PDN designs to minimize a cost function that penalizes impedance violations and component count. While capable of finding global optima in nonlinear solution spaces, they are computationally expensive. Pole-Zero Method is a deterministic approach that exploits the physics of the PDN^[4]. It identifies impedance peaks (poles) in the bare board response and selects capacitors with SRFs (zeros) that align with these frequencies.

$$\min|\Delta f| = |f_{\text{peak}} - f_{\text{SRF}}| \quad (3)$$

Research indicates that P&Z yields results comparable to GA but with significantly higher computational efficiency, making it ideal for initial design centering.

IV. THE PCB-PACKAGE RESONANCE & THE "51ST DECAP" PARADOX

The most critical discontinuity in modern PDNs is the interface between the inductive PCB (L_{PCB}) and the capacitive package (C_{PKG}). This forms a parallel RLC tank resonating between 10 MHz and 100 MHz.

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{PCB}} \cdot C_{\text{Total_PKG}}}} \quad (4)$$

The magnitude of this peak is determined by the Quality Factor ($Q \approx 1/R * (L/C)^{1/2}$). This relationship highlights the "51st Decap" Paradox. In a brute-force attempt to lower impedance, designers may add more high-quality (low-ESR) capacitors. If the reduction in damping resistance (R) is more drastic than the reduction in inductance (L), the Q factor increases. Consequently, adding a capacitor can worsen voltage ripple by sharpening the resonant peak. Mitigation Strategy: The goal is not to eliminate the peak but to damp it ($Q < 0.64$). This requires a "Controlled ESR" strategy, where capacitors are selected not just for capacitance but for specific ESR values that provide critical damping to the system.

V. ADVANCED TECHNOLOGIES AND CO-DESIGN

Reversed Aspect Ratio (LW) capacitors to combat the physical limit of inductance, reversed LW capacitors (e.g., 0204 size) utilize terminations on the long side of the device. This geometry shortens the current path and widens the conductor, reducing Equivalent Series Inductance (ESL) from ~ 500 pH (standard 0402) to ~ 70 pH. However, this benefit is realized only if the mounting loop inductance is minimized via optimized stack-ups (placing power planes on upper layers). Traditional board-only optimization treats the package as a passive load, leading to massive overdesign. A study from DesignCon 2023^[5] demonstrated that optimizing a board in isolation required 44 capacitors to suppress high-frequency noise. When the package model (including on-package decaps) was included in the simulation, the optimizer recognized that the package already handled the high frequencies. The board requirement dropped to 4 capacitors, a 10x reduction in component count.

VI. CASE STUDY: ACHIEVING 4 M Ω TARGET

We analyze a design challenge for a 1.2V core rail with a strict 4 m Ω target impedance ($I_{\text{AC}} = 3\text{A}$, $V_{\text{ripple}} < 24\text{mV}$). Initial State: The design failed due to a high Q resonance at the PCB-Package interface. Stack-up Optimization: The main power plane was moved from layer V11 to V04, reducing mounting via inductance by 30%.

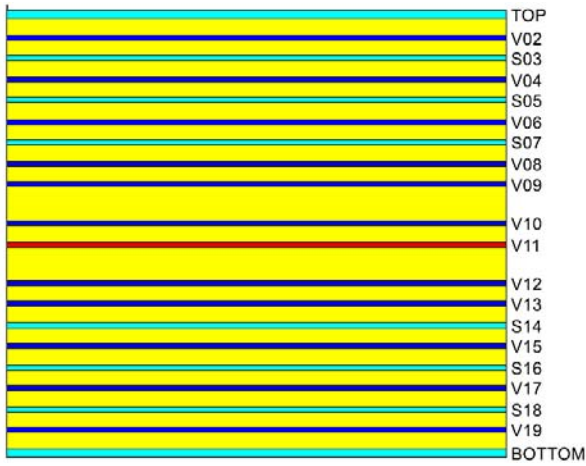


Fig. 4. 20 Layer PCB stack up

Component Selection: Standard 0402 capacitors were replaced with reversed LW (0204) capacitors to lower the inductive floor. **Damping:** Utilizing the "51st Decap" analysis, specific capacitors were chosen to maintain sufficient ESR for damping.

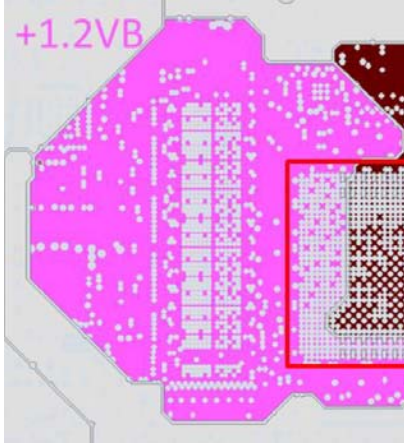


Fig. 5. Dynamic copper power plane powering BGA package IC

Package Integration: On-package capacitance was doubled to 12 μF , effectively shielding the PCB from the highest-frequency transients.

TABLE I
Simulation parameters

Metric	Composition	Result
Homogenous	30x 22uF (Low ESR)	95.95 m Ω (FAIL)
Optimized	Mix: 22uF, 4.7uF, 1uF	84.02 m Ω (PAsS)

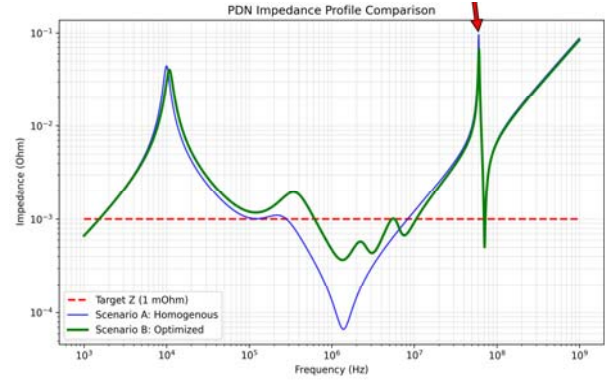


Fig. 6. PDN Impedance Profile Comparison

Result: The co-design approach met the 4 m Ω target with a minimal component footprint, validating the methodology.

VII. CONCLUSION

This research establishes that achieving sub-milliohm impedance requires a holistic strategy transcending the PCB boundary. Key takeaways include: Inductance is the primary limiter. No amount of capacitance can fix a violation of the physical inductance limit ($L_{\text{PCB_IC}} \parallel L_{\text{above}}$). Co-design is mandatory. Board-level optimization without package models leads to gross over-design. Resonance management over suppression. The optimal strategy is to damp the PCB-Package resonance ($Q < 0.64$) through a balance of reduced L (LW caps), increased C (package caps), and controlled R (ESR). By adopting these physics-based strategies, engineers can design PDNs that are robust, cost-effective, and manufacturable.

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